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PALCE20V8

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

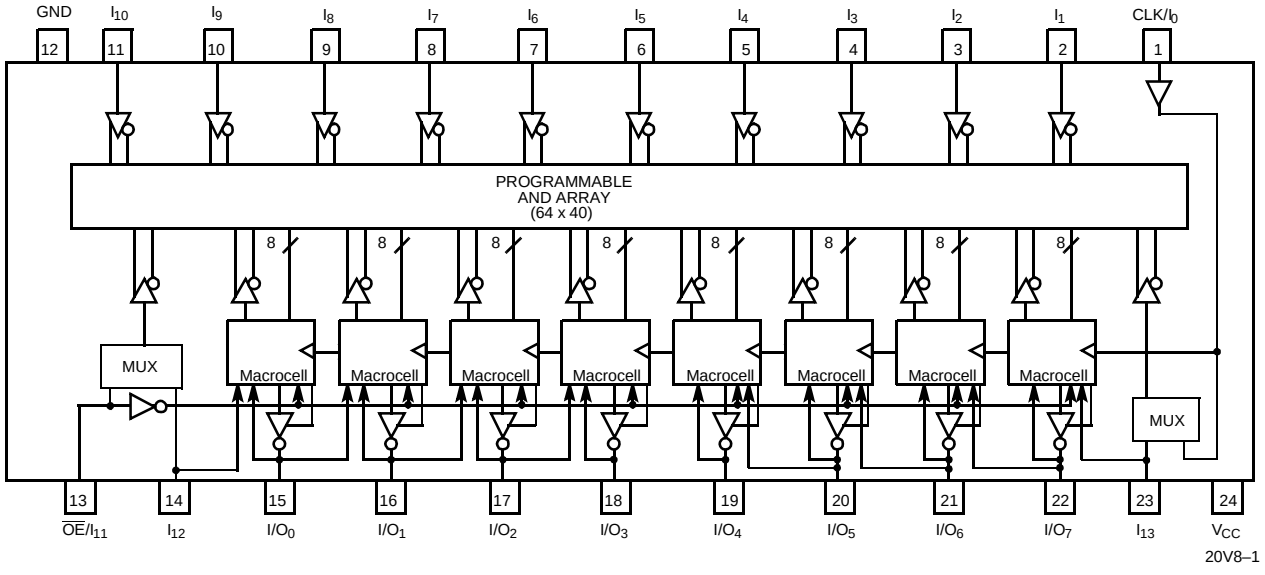
- **Active pull-up on data input pins**
- **Low power version (20V8L)**
  - **—55 mA max. commercial (15, 25 ns)**
  - **—65 mA max. military/industrial (15, 25 ns)**
- **Standard version has low power**
  - **—90 mA max. commercial (15, 25 ns)**
  - **—115 mA max. commercial (10 ns)**
  - **—130 mA max. military/industrial (15, 25 ns)**
- **CMOS Flash technology for electrical erasability and reprogrammability**
- **User-programmable macrocell**
  - **—Output polarity control**
  - **—Individually selectable for registered or combinatorial operation**
- **QSOP package available**
  - **—10, 15, and 25 ns com'l version**
  - **—15, and 25 ns military/industrial versions**
- **High reliability**
  - **—Proven Flash technology**
  - **—100% programming and functional testing**

Functional Description

The Cypress PALCE20V8 is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

The PALCE20V8 is executed in a 24-pin 300-mil molded DIP, a 300-mil cerdip, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and a 24-lead quarter size outline. The device provides up to 20 inputs and 8 outputs. The PALCE20V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 24-pin PLDs such as 20L8, 20R8, 20R6, 20R4.

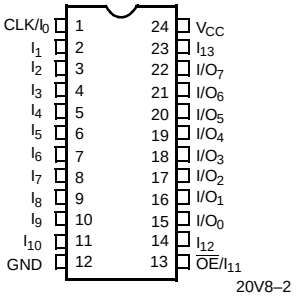
Logic Block Diagram (PDIP/CDIP/QSOP)



PAL is a registered trademark of Advanced Micro Devices, Inc.

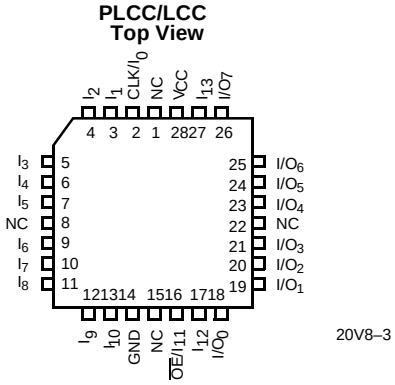
Pin Configuration

DIP/QSOP
Top View



20V8–2

PLCC/LCC
Top View



20V8–3

Selection Guide

Generic Part Number	t_{PD} ns		t_S ns		t_{CO} ns		I_{CC} mA	
	Com'l/Ind	Mil	Com'l/Ind	Mil	Com'l/Ind	Mil	Com'l	Mil/Ind
PALCE20V8–5	5		3		4		115	
PALCE20V8–7	7.5		7		5		115	
PALCE20V8–10	10	10	10	10	7	10	115	130
PALCE20V8–15	15	15	12	12	10	12	90	130
PALCE20V8–25	25	25	15	20	12	20	90	130
PALCE20V8L–15	15	15	12	12	10	12	55	65
PALCE20V8L–25	25	25	15	20	12	20	55	65

Shaded area contains preliminary information.

Functional Description (continued)

The PALCE20V8 features 8 product terms per output and 40 input terms into the AND array. The first product term in a macrocell can be used either as an internal output enable control or as a data product term.

There are a total of 18 architecture bits in the PALCE20V8 macrocell; two are global bits that apply to all macrocells and 16 that apply locally, two bits per macrocell. The architecture bits determine whether the macrocell functions as a register or combinatorial with inverting or noninverting output. The output enable control can come from an external pin or internally from a product term. The output can also be permanently enabled, functioning as a dedicated output or permanently disabled, functioning as a dedicated input. Feedback paths are selectable from either the input/output pin associated with the macrocell, the input/output pin associated with an adjacent pin, or from the macrocell register itself.

Power-Up Reset

All registers in the PALCE20V8 power-up to a logic LOW for predictable system initialization. For each register, the associated output pin will be HIGH due to active-LOW outputs.

Electronic Signature

An electronic signature word is provided in the PALCE20V8 that consists of 64 bits of programmable memory that can contain user-defined data.

Security Bit

A security bit is provided that defeats the readback of the internal programmed pattern when the bit is programmed.

Low Power

The Cypress PALCE20V8 provides low-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

Product Term Disable

Product Term Disable (PTD) fuses are included for each product term. The PTD fuses allow each product term to be individually disabled.

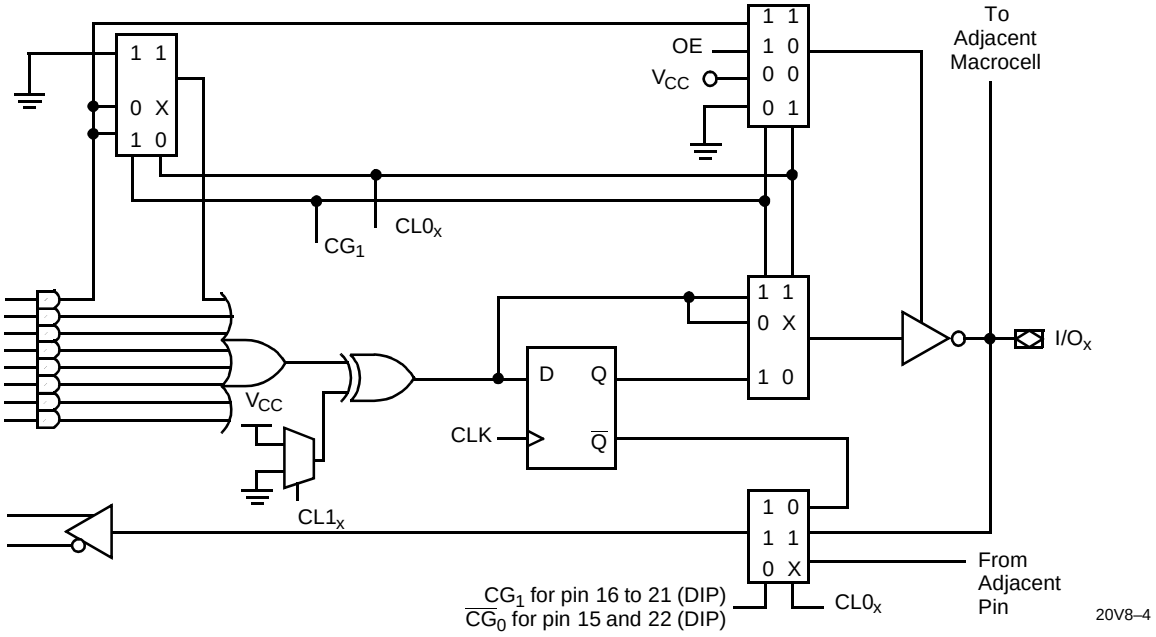
Input and I/O Pin Pull-Ups

The PALCE20V8 input and I/O pins have built-in active pull-ups that will float unused inputs and I/Os to an active HIGH state (logical 1). All unused inputs and three-stated I/O pins should be connected to another active input, V_{CC}, or Ground to improve noise immunity and reduce I_{CC}.

Configuration Table

CG_0	CG_1	$CL0_X$	Cell Configuration	Devices Emulated
0	1	0	Registered Output	Registered Med PALs
0	1	1	Combinatorial I/O	Registered Med PALs
1	0	0	Combinatorial Output	Small PALs
1	0	1	Input	Small PALs
1	1	1	Combinatorial I/O	20L8 only

Macrocell



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

Output Current into Outputs (LOW)..... 24 mA

DC Programming Voltage..... 12.5V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Industrial	–40°C to +85°C	5V ±10%
Military[1]	–55°C to +125°C	5V ±10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	Com'l	2.4		V
			I_{OH} = –2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}[4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			–0.5	0.8	V
I_{IH}	Input or I/O HIGH Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}				10	µA
I_{IL}[5]	Input or I/O LOW Leakage Current	0V ≤ V_{IN} ≤ V_{IN} (Max.)				–100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[6,7]			–30	–150	mA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., V_{IL} = 0V, V_{IH} = 3V, Output Open, f = 15 MHz (counter)	5, 7, 10 ns	Com'l		115	mA
			15, 25 ns			90	mA
			15L, 25L ns			55	mA
			10, 15, 25 ns	Mil/Ind		130	mA
			15L, 25L ns	Mil/Ind		65	mA

Capacitance[7]

Parameter	Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz	5	pF

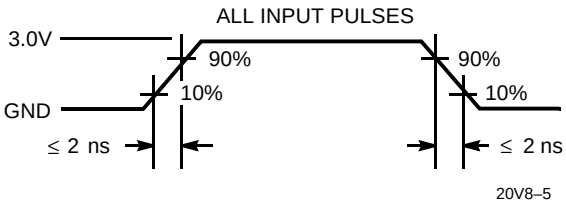
Endurance Characteristics[7]

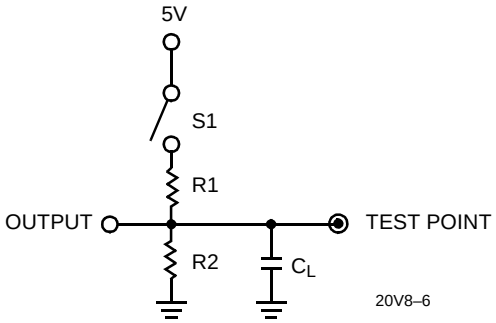
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to −3.0V for pulse durations less than 20 ns.
5. The leakage current is due to the internal pull-up resistor on all pins.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t_{PZX}, t_{EA}	Z ◗ H: Open Z ◗ L: Closed						1.5V
t_{PXZ}, t_{ER}	H ◗ Z: Open L ◗ Z: Closed	5 pF					H ◗ Z: V_{OH} – 0.5V L ◗ Z: V_{OL} + 0.5V

Commercial and Industrial Switching Characteristics[2]

Parameter	Description	20V8–5		20V8–7		20V8–10		20V8–15		20V8–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]	1	5	1	7.5	1	10	1	15	1	25	ns
t_{PZX}	$\overline{OE}$ to Output Enable		5		6		10		15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable		5		6		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]		6		9		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7,9]		6		9		10		15		25	ns
t_{CO}	Clock to Output Delay[8]	1	4	1	5	1	7	1	10	1	12	ns
t_S	Input or Feedback Set-Up Time	3		7		10		12		15		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	7		12		17		22		27		ns
t_{WH}	Clock Width HIGH[7]	3		5		8		8		12		ns
t_{WL}	Clock Width LOW[7]	3		5		8		8		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[7,10]	143		83		58		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 11]	166.6		100		62.5		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[7,12]	166.6		100		62.5		50		40		MHz
t_{CF}	Register Clock to Feedback Input[7, 13]		3		3		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		1		1		µs

Shaded area contains preliminary information.

Notes:

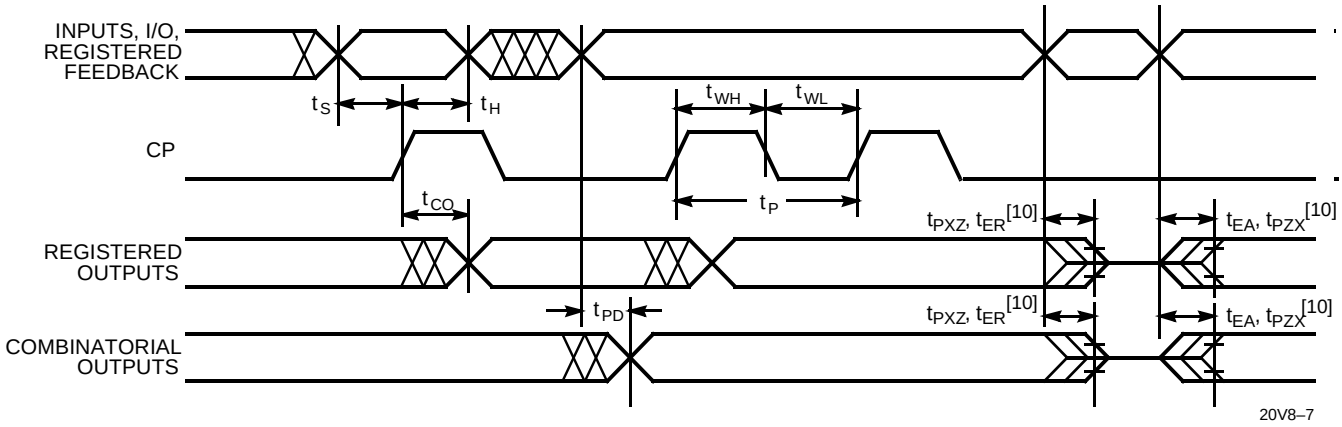
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This parameter is measured as the time after $\overline{OE}$ pin or internal disable input disables or enables the output pin. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
13. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 7 above) minus t_S.

Military Switching Characteristics[2]

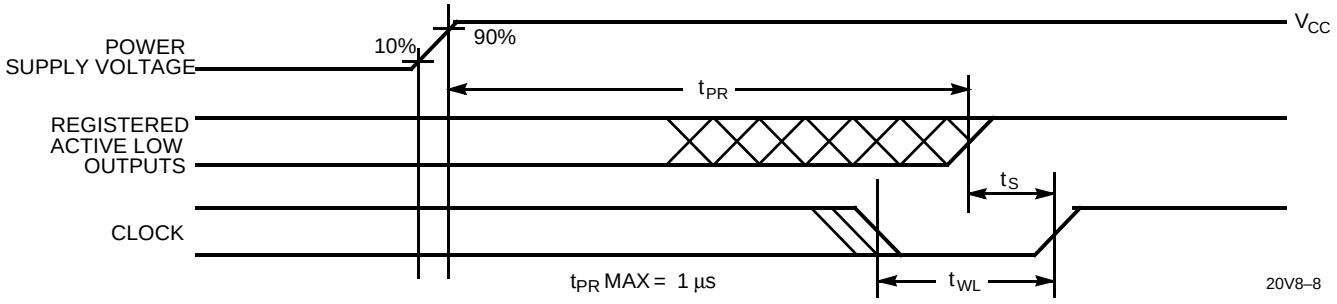
Parameter	Description	20V8–10		20V8–15		20V8–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]	1	10	1	15	1	25	ns
t_{PZX}	$\overline{OE}$ to Output Enable		10		15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7,9]		10		15		25	ns
t_{CO}	Clock to Output Delay[8]	1	10	1	12	1	20	ns
t_S	Input or Feedback Set-Up Time	10		12		20		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	20		24		40		ns
t_{WH}	Clock Width HIGH[7]	8		10		15		ns
t_{WL}	Clock Width LOW[7]	8		10		15		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[7,10]	50		41.7		25		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 11]	62.5		50		33.3		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[7,12]	62.5		50		33.3		MHz
t_{CF}	Register Clock to Feedback Input[7, 13]		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		µs

Shaded area contains preliminary information.

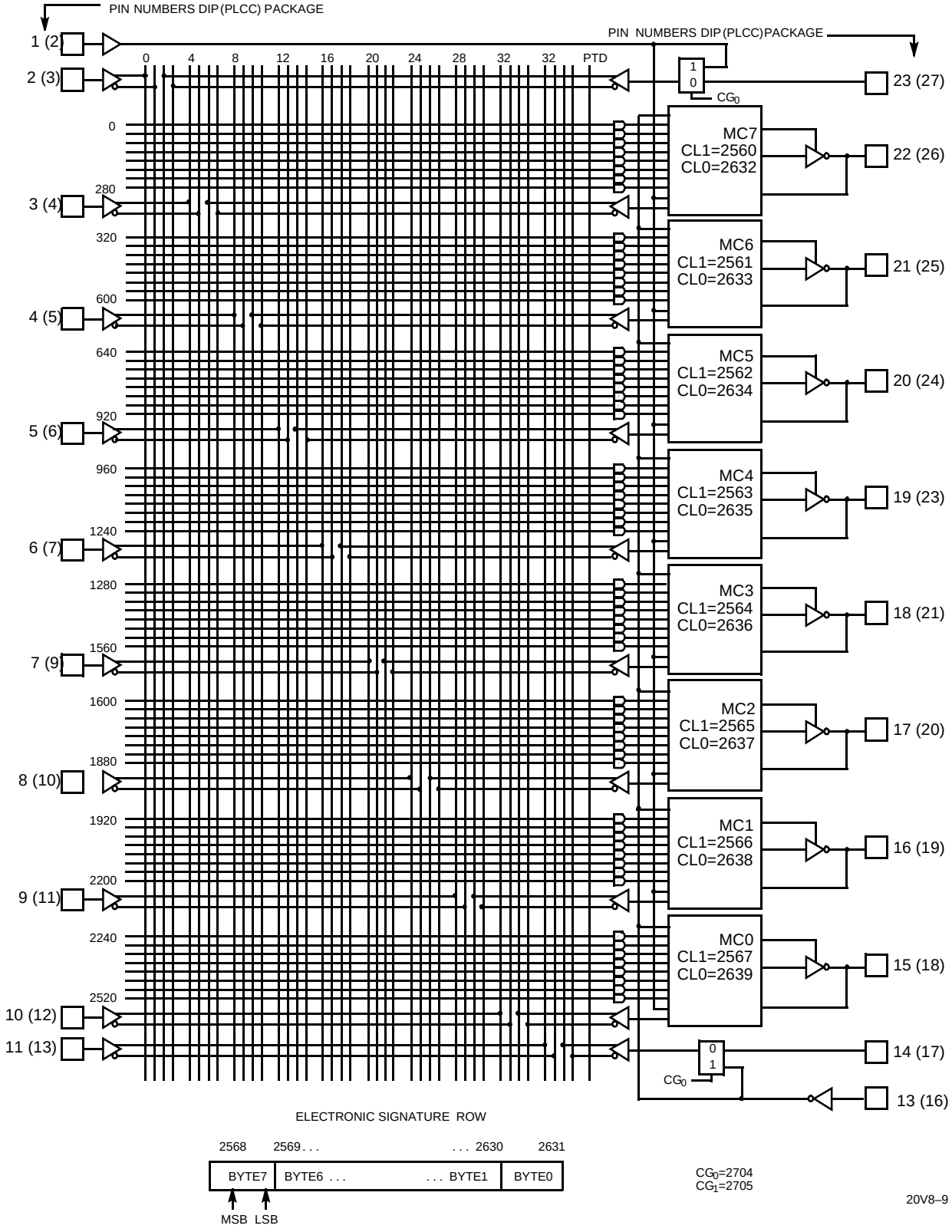
Switching Waveform



Power-Up Reset Waveform



Functional Logic Diagram for PALCE20V8



Ordering Information for PALCE20V8

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
115	5	3	4	PALCE20V8–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
115	7.5	7	5	PALCE20V8–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE20V8–7PC	P13	24-Lead (300-Mil) Molded DIP	
115	10	10	7	PALCE20V8–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PALCE20V8–10PC	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–10QC	Q13	24-Lead Quarter-Size Outline	
130	10	10	10	PALCE20V8–10JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE20V8–10PI	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALCE20V8–10LMB	L64	28-Pin Square Leadless Chip Carrier	
90	15	12	10	PALCE20V8–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE20V8–15PC	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–15QC	Q13	24-Lead Quarter-Size Outline	
130	15	12	12	PALCE20V8–15JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE20V8–15PI	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–15QI	Q13	24-Lead Quarter-Size Outline	
				PALCE20V8–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALCE20V8–15LMB	L64	28-Pin Square Leadless Chip Carrier	
90	25	15	12	PALCE20V8–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE20V8–25PC	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–25QC	Q13	24-Lead Quarter-Size Outline	
130	25	20	20	PALCE20V8–25JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE20V8–25PI	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8–25QI	Q13	24-Lead Quarter-Size Outline	
				PALCE20V8–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALCE20V8–25LMB	L64	28-Pin Square Leadless Chip Carrier	

Shaded area contains preliminary information.

Ordering Information for PALCE20V8L

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	15	12	10	PALCE20V8L–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE20V8L–15PC	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8L–15QC	Q13	24-Lead Quarter-Size Outline	
65	15	12	12	PALCE20V8L–15JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE20V8L–15PI	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8L–15QI	Q13	24-Lead Quarter-Size Outline	
				PALCE20V8L–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALCE20V8L–15LMB	L64	28-Pin Square Leadless Chip Carrier	
55	25	15	12	PALCE20V8L–25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE20V8L–25PC	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8L–25QC	Q13	24-Lead Quarter-Size Outline	
65	25	20	20	PALCE20V8L–25JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE20V8L–25PI	P13	24-Lead (300-Mil) Molded DIP	
				PALCE20V8L–25QI	Q13	24-Lead Quarter-Size Outline	
				PALCE20V8L–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALCE20V8L–25LMB	L64	28-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3

DC Characteristics

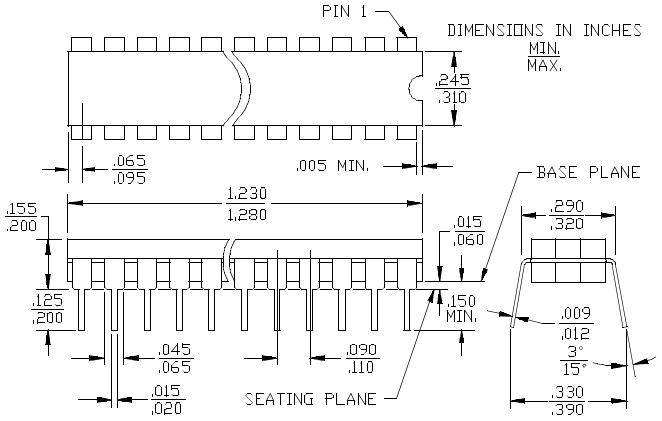
Parameter	Subgroups
I_{CC}	1, 2, 3

Switching Characteristics

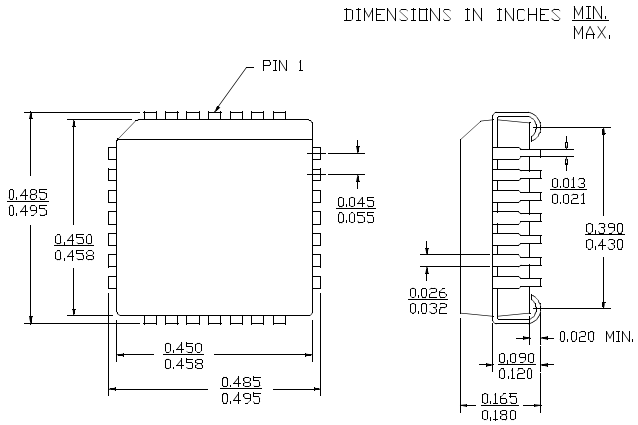
Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Package Diagrams

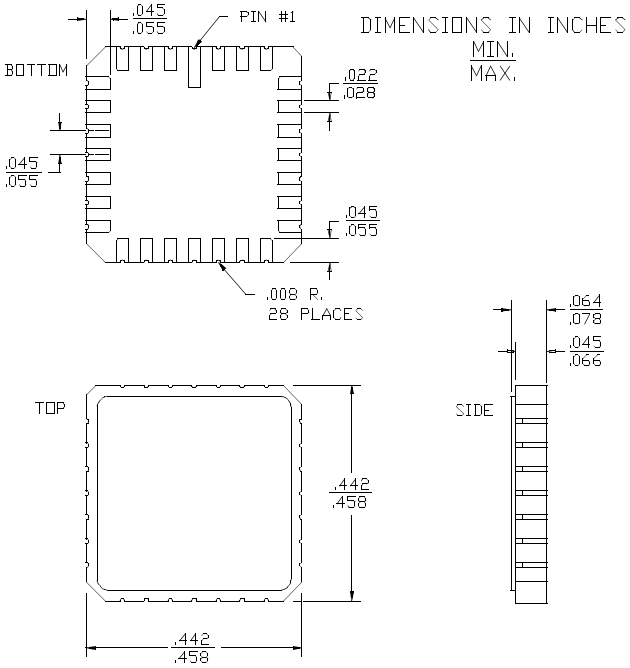
24-Lead (300-Mil) CerDIP D14
MIL–STD–1835 D–9 Config.A



28-Lead Plastic Leaded Chip Carrier J64

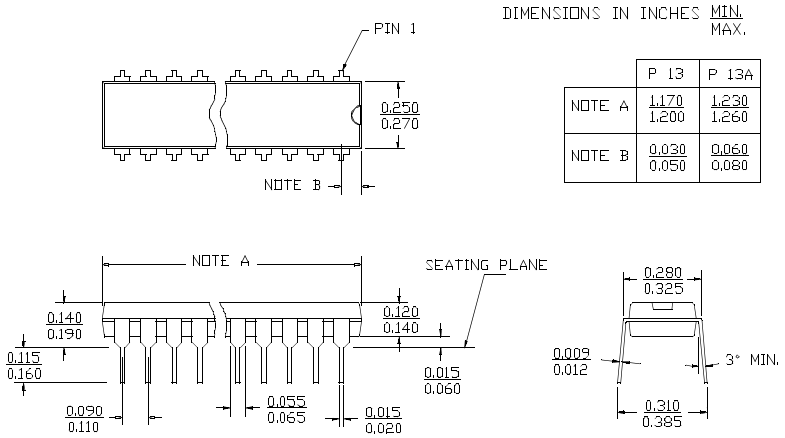


28-Square Leadless Chip Carrier L64
MIL–STD–1835 C–4



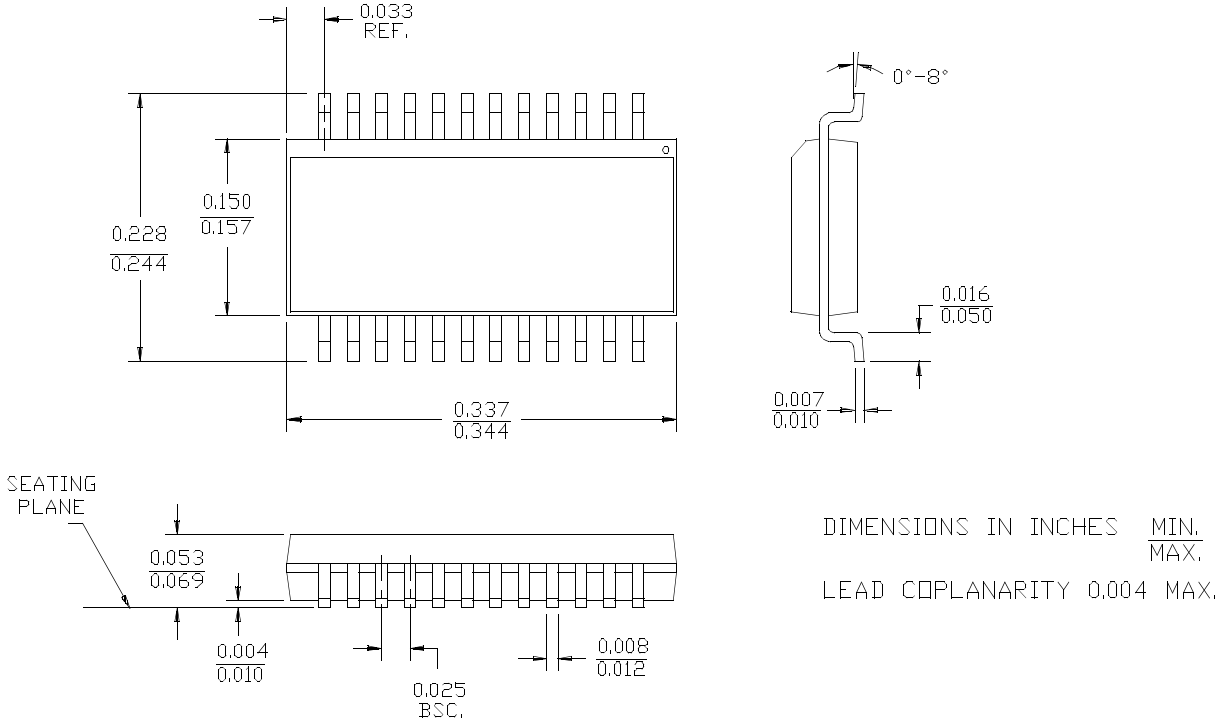
Package Diagrams (continued)

24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

24-Lead Quarter Size Outline Q13



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106371	07/11/01	SZV	Change from Spec Number: 38-00367 to 38-03026

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